L Number	Hits	Search Text	DB	Time stamp
1	722	438/230-232.ccls.	USPAT; US-PGPUB	2003/03/05 14:09
2	72	438/230-232.ccls. and (width with sidewall$)	USPAT; US-PGPUB	2003/03/05 14:16
3	39	(438/230-232.ccls. and (width with sidewall$)) and plasma	USPAT; US-PGPUB	2003/03/05 13:57
4	1732	257/350,351,369.ccls.	USPAT; US-PGPUB	2003/03/05 14:06
5	41	257/350,351,369.ccls. and (width with sidewall$)	USPAT; US-PGPUB	2003/03/05 14:06
6	32	(257/350,351,369.ccls. and (width with sidewall$)) not (438/230-232.ccls. and (width with sidewall$))	USPAT; US-PGPUB	2003/03/05 14:05
8	945	257/350,351,369.ccls.	EPO; JPO; DERWENT	2003/03/05 14:07
10	47	257/350,351,369.ccls. and PMOS and NMOS	EPO; JPO; DERWENT	2003/03/05 14:13
13	7	PMOS and NMOS and (sidewall$ same width)	EPO; JPO; DERWENT	2003/03/05 14:15
14	423	PMOS and NMOS and (sidewall$ same width)	USPAT; US-PGPUB	2003/03/05 14:15
15	392	(PMOS and NMOS and (sidewall$ same width)) not (438/230-232.ccls. and (width with sidewall$))	USPAT; US-PGPUB	2003/03/05 14:16
16	383	((PMOS and NMOS and (sidewall$ same width)) not (438/230-232.ccls. and (width with sidewall$))) not (257/350,351,369.ccls. and (width with sidewall$))	USPAT; US-PGPUB	2003/03/05 14:16

US-PAT-NO: 6316304

DOCUMENT-IDENTIFIER: US 6316304 B1

TITLE: Method of forming spacers of multiple widths

---------- KWIC ---------

The invention generally relates to an interconnection process used in semiconductor manufacturing and, more particularly, to a method of forming different **width sidewall** spacers in the fabrication of integrated circuits.

Referring now to FIG. 2, the spacer oxide layer 18 is partially etched away. A portion of the spacer oxide layer 18 remains along the **sidewalls** of the gate structure 12/14 forming equal **width** spacers beside the gate. A subsequent implantation (not shown) creating the more heavily doped source and drain (S/D) regions 20 is masked by the sidewall spacers.

In order to mix transistors from different process technologies or with different operating voltages, it is desirable to have different LDD widths for PMOS and NMOS transistors. The **width** of the LDD region is typically controlled by the **width** of the gate **sidewall** spacers. Other approaches for forming different spacer widths exist. U.S. Pat. No. 5,021,354 to Pfiester teaches a method that takes advantage of variation in oxidation of regions with different dopants to form spacers of differing widths. U.S. Pat. No. 5,405,791 to Ahmad et al. teaches a method where equal width spacers are formed. The PMOS device is then masked and an n+ source/drain (S/D) implantation is performed in

the NMOS device. The mask is removed and additional oxide is deposited. The NMOS device is then masked and the oxide etched to form the optimal spacer width on the PMOS device. A p+ implantation then forms the S/D regions in the PMOS device. The spacers are then removed and the lightly doped source/drain (LDD) extensions are implanted. Unfortunately, the Ahmad invention cannot be adapted to a self-aligned silicide (salicide) metalization process since the completed device has a covering of silicon nitride. In addition, it has the limitation of only facilitating different spacer widths between NMOS and PMOS devices. U.S. Pat. No. 5,460,998 to Liu teaches a method similar to Ahmad except that the LDD extensions are implanted prior to forming the spacers.

U.S. Pat. No. 5,424,572 to Solheim teaches a method that takes advantage of the 8:1 ratio of oxide growth over n+ and p+ regions, respectively. The oxide is grown and then etched, leaving spacers only along the n+ doped sidewalls.

U.S. Pat. No. 5,786,247 to Chang et al. teaches a method where spacers are formed in separate steps over the NMOS and PMOS regions allowing individual adjustment of the LDD profiles. U.S. Pat. No. 5,874,330 to Ahn teaches a method where nitride caps are formed over selected devices. The surface is covered with oxide, which is then etched, allowing selective LDD implantation.

These objects are achieved using a process where the gate structure, comprising a gate dielectric covered by a gate electrode, is formed by conventional techniques upon a substrate. An implantation is performed to form LDD regions in the substrate not protected by the gate structure. The exposed substrate and gate structure are then covered with an insulating liner layer and an etch

stop layer. A thin spacer oxide layer is then deposited over the etch stop layer. Areas where ticker spacers are desired are masked and the unmasked spacer oxide layer is removed. The mask is then stripped away and additional spacer oxide layer is grown over the surface. The result is a thicker spacer oxide layer in areas protected by the mask during the previous etching. The spacer oxide layer is then anisotropically etched forming spacers along the gate sidewalls. The spacers are wider in the areas with the thicker oxide. The process continues by etching away the etch stop layer not protected by the spacers. Adjustment of the spacer width is accomplished by varying the total thickness of the etch stop and spacer oxide layers. Adjustment of the difference in spacer **width** is controlled by the thickness of the first spacer oxide deposition The process is completed by implanting the substrate in areas not protected by the gate structure and **sidewall** spacers to form the source and drain (S/D).

The preferred embodiment describes formation of sidewall spacers on gate structure sidewalls to be used to mask a subsequent source/drain (S/D) implantation. While this embodiment describes spacers along the **sidewalls** of a gate electrode, it will be understood by those skilled in the art that the invention can be extended to the formation of different **width** spacers on any structure on a semiconductor wafer.

Referring now to FIG. 7, the exposed etch stop layer is etched away using a **plasma** etch process with a chemistry of SF.sub.4 /HBr or CF.sub.4 /HBr, thereby completing the spacer formation. Two different spacer widths (w and W) are shown along the sidewalls of the gate structures 32/34 and

32/35 of transistor
46 and transistor 48. The typical difference in widths between W and w (W-w)
are between about 100 to 400 Angstroms.

anisotropically etching a portion of said first oxide layer and said second
oxide layer to said etch stop layer thereby forming spacers along the **sidewalls**
of said first and second device structures wherein said spacers on **sidewalls** of
said second device structure have a **width** greater than the **width** of said
spacers on **sidewalls** of said first device structure; and

9. The method according to claim 1 wherein said etching away of said etch stop
layer is performed using a **plasma** etch process with a chemistry of SF.sub.4
/HBr or CF.sub.4 /HBr.

anisotropically etching a portion of said first oxide layer and said second
oxide layer to said etch stop layer thereby forming spacers along the **sidewalls**
of said first and second gate structures wherein said spacers on **sidewalls** of
said second gate structure have a **width** greater than the **width** of said spacers
on **sidewalls** of said first gate structure;

18. The method according to claim 10 wherein said etching away of said etch
stop layer is performed using a **plasma** etch process with a chemistry of
SF.sub.4 /HBr or CF.sub.4 /HBr.

anisotropically etching a portion of said first oxide layer and said second
oxide layer to said etch stop layer thereby forming spacers along the **sidewalls**
of said PMOS and NMOS gate structures wherein said spacers on **sidewalls** of said
NMOS gate structure have a **width** greater than the **width** of said spacers on
sidewalls of said PMOS gate structure;

27. The method according to claim 19 wherein said etching away of said etch
stop layer is performed using a **plasma** etch process with a chemistry of
SF.sub.4 /HBr or CF.sub.4 /HBr.

US-PAT-NO: 5688722

DOCUMENT-IDENTIFIER: US 5688722 A

TITLE: CMOS integrated circuit with reduced susceptibility to PMOS
punchthrough

---------- KWIC ---------

1.) The starting wafer is a (100) oriented wafer, doped N-type to a resistivity
of about 20 to 40 ohm-centimeters. After clean-up, an initial oxide is grown
to about 950 .ANG.ngstroms, and about 1,500 .ANG.ngstroms of silicon nitride is
then deposited over the oxide. Photoresist is then deposited, and patterned
according to the N-well pattern. Exposed portions of the nitride are then
etched away by **plasma** etching, and phosphorus is implanted to dope the N-well.
In this sample embodiment, phosphorous is implanted at 175 keV at a dosage of
8.5.times.10.sup.12 cm.sup.-2. A first field oxide is then grown to about
5,500 .ANG.ngstroms. (Note that this field oxide will grow generally in places
which were exposed by the N-well mask, where phosphorous was implanted.) The
remaining silicon nitride is then cleared, and boron is implanted to dope the
P-well areas. (The first field oxide, which is thick over the N-well areas,
will keep this implant out of the N-well areas.) In this sample embodiment, the
P-well boron dose is 5.0.times.10.sup.12 at 100 keV. A long high-temperature
drive step will then be performed to drive in the N-well and P-well dopings
(for example about 250 minutes at about 1150 degrees C). The first field oxide
is then stripped. This completes the formation of the

N-well and P-well
regions, in which the PMOS and NMOS active devices (respectively) will be
formed. The resulting junction depth of the P-wells will be about 4 microns.
The added doping of the N-type wells will taper off into the substrate doping
at about the same depth.

2.) The active device areas will now be fabricated. First, a pad oxide is
grown, to about 600 .ANG.Angstroms, and nitride is deposited, to about 1,500
.ANG.ngstroms. Photoresist is deposited and patterned, so that the areas where
active devices will be desired are covered, and remaining areas are exposed. A
plasma etch is now used to strip the nitride from these areas. The photoresist
is now stripped, and another layer of photoresist is deposited and patterned to
expose only the regions where channel stops for the NMOS devices are desired.
Boron is now implanted, e.g. at 30 keV at a dosage of 1.1.times.10.sup.14 per
centimeter squared, and the photoresist is then stripped, A high temperature
oxidation is now performed, to grow field isolation oxide to a thickness of
about 5,900 .ANG.Angstroms. A **plasma** etch now removes the remaining silicon
nitride portions.

One example of variation is in the **width of the sidewall** oxide filaments
(which, together with the diffusion length of the some/drain doping, defines
the offset of the source/drain regions from the gate comers. The width of
these filaments can be adjusted, within limits, by changing the thickness of
the conformal oxide deposition, and/or by changing the degree of overetch used
after the conformal oxide is cleared, and/or by performing multiple conformal
deposition and etchback steps. Thus, the width of these spacers can readily be

adjusted. The only limits on this adjustment are provided by the functionality described above: if the **sidewall** oxide **width** is reduced too far, the relatively light concentration of the lateral field isolating regions could be swamped by the lateral diffusion from the source/drain regions. Conversely, if the sidewall oxide were made extremely wide (e.g. by multiple filaments), to the point where some portions of the lateral field isolating regions were not well coupled to the fringing fields at the gate corners, the threshold voltage of the PMOS devices would be increased.

US-PAT-NO: 5399514

DOCUMENT-IDENTIFIER: US 5399514 A

TITLE: Method for manufacturing improved lightly doped diffusion (LDD)
semiconductor device

---------- KWIC ---------

It is difficult, however, to control the **width of sidewalls** 31 to have a
uniform film thickness, or a target film thickness, over the entire surface of
a 5-inch or 6-inch semiconductor wafer. A variety of processing methods are
used in the prior art to form sidewalls 31, including low-pressure, **plasma**
formation, and atmospheric pressure methods. Any of these methods typically
has a.+-.20% variation in target film thickness and a.+-.15% variation in
coverage across the wafer. Within a single wafer, the variation can commonly
run as high as 900 .ANG., for a 3000 .ANG. thick film. Between wafers in a
lot, there can be as much as a 1200 .ANG. variation.

A **sidewall** 31 made with film thicknesses subject to large variations will also
show large variations in **width**. And if the width varies, then the lengths of
the p-type first and n-type diffusion layers will likewise vary. This
variation will appear as an uncontrolled variation in channel resistance for
the affected transistors. The obvious result consequence is variations will be
produced in transistor performance. As circuit geometries continue to get even
finer with the advancing state-of-the-art, the channel length under the gates
gets shorter, and the variations in series resistance gets

more pronounced. As
such, the above problem can limit using smaller device geometries, because
device yields fall to unacceptable levels.

US-PAT-NO: 4978626

DOCUMENT-IDENTIFIER: US 4978626 A

TITLE: LDD transistor process having doping sensitive endpoint etching

---------- KWIC ---------

Processes which implement lightly doped drain (LDD) structures are well known. Accordingly, reasons for using and advantages of the lightly doped drain structure are well documented. The conventional LDD process involves formation of gate sidewall spacers. A lightly doped drain region is typically implanted into a substrate prior to the formation of a sidewall spacer. The sidewall spacer is commonly formed by depositing a dielectric after the gate is formed and anisotropically etching the dielectric to create the spacer. With the **sidewall** spacer is place, a heavy source/drain dopant is implanted with the gate and **sidewall** spacer acting as a mask to provide source and drain regions laterally displaced from the gate edges by the **width of the sidewall** spacer. The process just detailed typically requires two or more photolithographic masking steps. When photolithographic masking steps are minimized, substantial manufacturing cost savings may be realized.

where "m" is an integer between one and six inclusive, and "n" is an integer between one and four inclusive. The optical emissions from the **plasma** is filtered so that only the wavelengths associated with the SiF.sub.n species reaches a photodetector. Because the undoped polysilicon is less conductive

than the doped polysilicon, the SF.sub.6 **plasma** reacts more slowly when it reaches the undoped polysilicon layer 15. As the reaction slows down, the SiF.sub.n emissions decrease. In order to amplify the early endpoint signal, a second etchant gas can be added to the etch **plasma**. This gas is preferably a chlorinated freon compound, such as CFCl.sub.3. In the **plasma,** this gas can be added to the etch **plasma**. This gas is preferably a chlorinated freon compound, such as CFCl.sub.3. In the **plasma,** this gas dissociates into subfluorides and subchlorides of carbon, which react with the polysilicon to form volatile subfluorides and subchlorides of silicon as follows:

where w, x, y and z are integers between one and four, inclusive. The optical emissions from the **plasma** is sent through a second filter so that only the wavelengths associated with the CClx species reaches a second photodetector. As previously described, the reaction stated by equation two will also slow down when the etch **plasma** reaches the undoped polysilicon layer 15. In this case, however, the emission from the reactant CClx increases and reaches a maximum at the approximate midpoint of layer 15. By ratioing these two divergent emission signals, V.sub.SiFn /V.sub.CClx, the amplitude of the early endpoint signal can be significantly amplified. Therefore, the ratio of fluorine to chlorine emissions is magnified when etching between doped and undoped polysilicon layers and specific etch points between differing doped layers can be easily and accurately detected. This doping sensitive technique can also apply to a technique which is a chlorine based etch chemistry.

US-PAT-NO: 4577391

DOCUMENT-IDENTIFIER: US 4577391 A

TITLE: Method of manufacturing CMOS devices

---------- KWIC ---------

A CMOS semiconductor structure having insulation **sidewall** spacers whose **width** is selected independently for NMOS and PMOS devices. The width of the spacer is selected to reduce hot electron injection in the N channel device and to insure that the gate and source regions are aligned with or underlap the gate in the P channel device. A narrower spacer is used for the P channel device than for the N channel device which permits the formation of a P channel device having a threshold voltage less than 1 volt.

This invention relates to a complementary metal-oxide semiconductor (CMOS) structure having insulation sidewall spacers. In particular, the invention relates to a CMOS structure (and to the methods of making same) in which the **width** of the insulation **sidewall** spacers is selected independently for N channel and P channel devices.

Later work by Riseman and others shows that the relationship between the thickness of the conformal layer and the thickness (**width) of the sidewall** spacer is more complex than is stated in the '362 patent. In Abstract No. 233, Sidewall Spacer Technology, P. J. Tsang, J. F. Shepard, and J. Riseman, IBM Corporation, Hopewell Junction, N.Y., which is incorporated herein by reference, the authors determined that there are three

major factors that affect the final dimension and geometric configuration of an insulation sidewall spacer:

The results reported in Sidewall Spacer Technology are reproduced in FIGS. 5a and 5b. An examination of FIGS. 5a and 5b show that unless the aspect ratio R=h/d is kept larger than 1.0 and angle .phi. equals zero (i.e. a vertical step) the **width** w of the **sidewall** produced will always be smaller than the deposited film thickness, i.e., (w/d)<1. In addition, the variation of the width w caused by uncertainty of R, .phi., and overetch Oe will be larger if R.ltoreq.1.0 and .phi..gtoreq.0. It is suggested in **Sidewall** Spacer Technology that for most device applications a **sidewall** spacer having a **width** w that is as close as possible to the thickness d of the CVD layer is desired. For these purposes a vertical step and an aspect ratio of 1.5 is recommended, so that the width of the spacer is not sensitive to overetch, as shown in FIG. 5a.

Of importance, in all of the above prior art techniques for forming an insulating sidewall spacer, it is nowhere disclosed or suggested that such spacers be formed in CMOS devices. In particular, it is not disclosed or suggested that the **width** of the insulation **sidewall** spacer be selected independently for NMOS and PMOS devices within a CMOS semiconductor structure.

A layer of photoresist 25 is formed on second layer 24 and patterned by conventional techniques and the resulting structure is anisotropically etched to form structure 20 including multilayer stack 26 as shown in FIG. 7. The anisotropic etch is performed, for example, using **plasma** SF.sub.6. Structure

20 is then subjected to a **plasma** etch using CF.sub.4 or SF.sub.6 or a wet etch using HF:HNO.sub.3 :H.sub.2 O=1:60:60 in order to produce stack 27 shown in FIG. 8. In FIG. 8, second layer 24 is undercut by approximately 1000 to 2,500 .ANG. by the **plasma** etch or wet etch which etches second layer 24 at a slower rate than doped polycrystalline silicon layer 23. **Plasma** etchant CF.sub.4 or SF.sub.6 etches doped polycrystalline silicon layer 23 at a rate approximately twice as fast as second layer 24 when the second layer is tungsten silicide (WSi.sub.2)

The process steps described in FIGS. 7 and 8 can, if desired, be combined in a single step **plasma** etch. In one embodiment of this invention dual stack 27 is produced using a single step planar **plasma** etching system using SF.sub.6 as the main etching species.

Whether stack 27 is formed in one or two etching steps, the amount of undercut is easily controlled due to the known differential etch rates of the selected etchant on second layer 24 and on polycrystalline silicon layer 23. In one embodiment an overhang of approximately 1,200 .ANG. of tungsten silicide is provided by a single step planar **plasma** etching system using SF.sub.6 for approximately 1 minute. The etching characteristics of a dual layer consisting of silicide/polycrystalline-silicon is described in In Line **Plasma** Etch of Polysilicon and Molybdenum Silicide using SF.sub.6, P. Chang, et al., Kodak Microelectronics Seminar Proceedings, pp. 9-14, October 1980, which is incorporated herein by reference.

Next, the structure 60 is vertically etched to remove portions of oxide layers 61 and 22 to expose the doped source/drain regions 42 and

to form structure 70
having vertical sidewall oxide spacers 71 which fill the regions under the ends
of second layer 24 as shown in FIG. 11. The **width** W of the **sidewall** oxide
spacer 71 as measured near the base of the spacer as shown in FIG. 11 is
approximately 0.3 microns. In general the **width** of an insulation **sidewall**
spacer formed in accordance with the teachings of this invention depends on the
thickness of the conformal insulation layer, the differential etch rates of the
second layer 24 and the underlying polycrystalline silicon layer 23, the etch
time, and the over-etch time. Spacers having a width in the range of about
0.15 mm to 0.4 mm are produced by controlling these variables. The etchant
used in one embodiment is CHF.sub.3 :O.sub.2 which has a high selectivity for
etching insulating layer 22 as compared with silicon. For example, when
insulating layer 22 is SiO.sub.2 the ratio of the etch rates of layer 22 to
silicon is about 5:1 and when insulating layer 22 is silicon nitride, the ratio
of the etch rates of layer 22 to silicon is about 2.5:1.

First, the width, W, of the oxide spacer 71 (as measured near the bottom of
spacer 71 as shown in FIG. 11) is principally controlled using the method of
the present invention by controlling the degree of undercutting, which depends
on the differential etch rates for second layer 24 and underlying doped
polycrystalline silicon layer 23, the etch time, and the over etch time, and
the thickness of the conformal oxide layer. The **width** of the oxide spacer
formed by prior art methods depends on the geometric factors described in
Sidewall Spacer Technology above, including the aspect ratio of the pattern
step and the angle that the edge of the pattern step makes with the vertical,

as well as the thickness of the CVD layer and over-etch time.

Second, the **width,** W, of the oxide spacer (as measured near the bottom of the spacer 71) is less sensitive to over etch time of the RIE and to the thickness of the CVD layer 61 than prior art methods as exemplified in **Sidewall** Spacer Technology, above, due to the protective overhang of second layer 24 as shown in FIG. 11.

Third, Miller capacitance is reduced in transistors having sidewall spacers formed according to this invention. This is illustrated in FIGS. 16a and 16b. FIG. 16a shows an N channel transistor 140 formed using prior art sidewall spacers. The Miller capacitance between the right end 143 of the dual stack gate comprising layer 121 and doped polycrystalline layer 23 and the N.sup.- region 42 beneath end 143 is inversely proportional to the distance d between the bottom surface 23c of right end 143 and the surface 42a of N.sup.- region 42. A parallel statement is true for left end 142. On the other hand, when sidewall spacers 71 are formed in accordance with the present invention, the Miller capacitance between the right end 153 of layer 121 and the N.sup.- region 42 beneath end 153 is inversely proportional to the distance d' between the bottom surface 121c of layer 121 and the surface 42a of N.sup.- region 42. A parallel statement is true for left end 152 of layer 121. Since d' is greater than d by the thickness of layer 23, Miller capacitance is reduced as compared with the Miller capacitance provided by prior art structures. Of importance, it is neither disclosed nor suggested by Riesman or in co-pending U.S. patent application Ser. No. 6,595,796 that the **width** of the insulation

sidewall spacer be selected independently for NMOS and PMOS devices within a
CMOS semiconductor structure.

As explained below, applicants have discovered that certain parameters for NMOS
and PMOS devices in a CMOS integrated cirucit can be enhanced by constructing
sidewall spacers for NMOS devices having greater **width than sidewall** spacers
for PMOS devices within a CMOS integrated circuit.

A CMOS semiconductor structure is disclosed having insulation **sidewall** spacers
wherein the **width** of the spacers is selected independently for NMOS and PMOS
devices in the structure. For an N channel device, the width of the spacer is
selected to reduce hot electron injection. In the P channel device, a narrower
spacer is selected to prevent the gate and source regions from underlapping the
gate and to create a small overlap. This permits the formation of P channel
devices having a threshold voltage less than approximately one volt.

FIG. 4a shows the geometric quantities that determine **sidewall** spacer **width**
using prior art techniques.

A second vertical RIE is performed using CHF.sub.3 :O.sub.2 in order to form
relatively thick **sidewall** spacers 16 having a **width** at their base of
approximately 0.4 to 0.5 microns as shown in FIG. 23. The second vertical etch
removes that portion of the gate oxide 3 not protected by the gate 5 or
sidewalls 16. In those embodiments where the gate stack is a dual layer gate
stack as shown in FIG. 8, the **sidewall** spacers 16 have a **width** at their base of
approximately 4000 to 5000 .ANG.. Source/drain regions 17 are then formed in
selected portions of source/drain regions 7 by implanting an N type dopant such

as arsenic to produce a peak concentration of approximately 1.times.10.sup.20 atoms/cm.sup.3 in N.sup.+ source/drain regions 17 as shown in FIG. 24.

The importance of forming a relatively wide **sidewall** spacer 17 having a **width** of approximately 4000 to 5000 .ANG. for N channel devices is explained with reference to FIGS. 24 and 25. Due to the shielding effect of spacer 16 during implantation of N.sup.+ regions 17, wide spacers 16 provide a separation of the N.sup.+ regions 17 from the gate 5 and from the channel region 2a underneath the gate 5 by the lightly doped portions 7a of source/drain regions 7. This lateral separation is necessary in order to reduce hot-electron injection by lowering the peak electric field at the N-channel drain pinch-off region. A high electric field can generate "hot" electrons which overcome the potential barrier between silicon and silicon dioxide These hot electrons can be captured by the traps in the gate oxide which can cause the N channel threshold voltage to shift.

forming a first and a second **sidewall** spacer having a first selected **width** abutting the respective ends of said second gate;

forming a third and a fourth **sidewall** spacer having a second selected **width** abutting, the ends of said first gate;

DERWENT-ACC-NO: 1986-030248

DERWENT-WEEK: 198605

TITLE: Formation of semiconductor structures esp. a CMOS structure - having
insulation **sidewall** spacers of independently selected **widths for NMOS and PMOS**
devices

---------- KWIC ---------

Formation of semiconductor structures esp. a CMOS structure - having insulation
sidewall spacers of independently selected **widths for NMOS and PMOS** devices

FORMATION SEMICONDUCTOR STRUCTURE CMOS STRUCTURE INSULATE **SIDEWALL** SPACE
INDEPENDENT SELECT **WIDTH NMOS** DEVICE